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A Novel Cascaded Multilevel Inverter Structure using Reduced Power Electronic Elements

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***Abstract*—Multilevel converter is a power electronic system that synthesizes a desired output voltage from several levels of dc voltages as inputs. Recently, use of multilevel converters has been extended for medium and high-power applications such as industrial, electric vehicles, renewable energy systems, motor drives, flexible ac transmission systems, and so on. Conventional multilevel inverter topologies when used for higher levels require large number of power electronic components. The proposed topology uses a novel cascade structure with reduced number of switches. The switching pulses for the inverter switches are generated by sinusoidal pulse width modulation using FPGA. Using the proposed topology a 25 level inverter can be realized with reduced number of switches. The output waveform is near sinusoidal. Compared with conventional multilevel inverters, it requires less number of components to achieve same number of output levels. Overall THD is very low and thus the quality of output waveform is improved. Due to the use of fewer switches, optimized circuit layout and packaging is possible. Thus less cost is required to implement the proposed inverter.**

***Index Terms*— Multilevel inverter (MLI); Cascaded H-Bridge (CHB); Total Harmonic distortion (THD); Sinusoidal Pulse Width modulation (SPWM).**

I. INTRODUCTION

Multilevel converter is a power electronic system that synthesizes a desired output voltage from several levels of dc voltages as inputs. Recently, use of multilevel converters has been extended for medium and high-power applications such as industrial electric vehicle applications, renewable energy systems, motor drives, flexible ac transmission system, and so on. Generally, multilevel converters are classified into three classic structures: neutral point clamped (NPC) converter, flying capacitor (FC) converter, and cascade H-bridge converter (CHB). The unequal voltage sharing among series-connected capacitors is the main draw-back of the NPC converter. In addition, this structure needs a large number of clamping diodes for higher levels. The FC converter requires a great number of storage capacitors for higher output voltage levels, and the capacitors voltage balancing is difficult. The CHB converter is the most important structure among classical multilevel converters, because this structure needs fewer number of power electronic components. A CHB converter consists of several H-bridges with separate dc sources for each H-bridge. A new structure for the multilevel converter has been proposed. This structure reduces the number of components such as power

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electronic switches and dc voltage sources in comparison with a conventional CHB structure. This MLI help to achieve near sinusoidal output waveforms with reduced THD. As the number of output levels increase, harmonics decrease. The disadvantage of conventional MLI is that if more number of output levels are required, then more number of components are needed and due to this complexity increases in gate driver circuits. Using the proposed converter structure 25 level can be generated with reduced number of switches compared to conventional CHB converter and near sinusoidal waveform can be obtained with reduced THD.

II. Basic Cell of Proposed Multilevel inverter

The proposed topology contains minimum number of switches for generating same output levels as compared to conventional MLI. The proposed MLI's basic cell generates 5 output levels using 2 voltage sources and 5 switches with anti-parallel diodes. Figure shows the arrangement of these switches, where S1, S2, S3, S4 are arranged same as conventional H-bridge while S5 is added to increase output level by selecting appropriate voltage source.

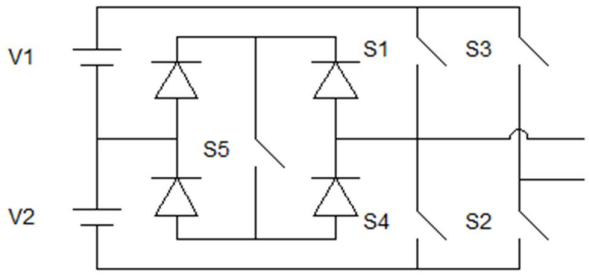

Fig. 1 Basic Cell of the Proposed Topology

The table is shown, regarding switching states of proposed MLI's basic cell where logic 'l' is considered as 'ON' state and logic' 0' is considered as' OFF' state of switch.

Table I. Switching States of Basic Cell

S1	S2	S3	S4	S5	OUTPUT VOLTAGE	OUTPUT VOLTAGE (IN Per Unit)
1	1	0	0	0	V1 + V2	1
0	1	0	0	1	V1	0.5
0	1	0	1	0	0	0
1	0	1	0	0	0	0
0	0	1	0	1	-V2	0.5
0	0	1	1	0	-(V1 + V2)	1

III. Proposed 25 Level Inverter

The proposed topology of multilevel inverter is employed by cascaded arrangement of two basic cells. Here the figure shows MLI where 25 output levels are obtained by using only 10 switches. This arrangement can be further augmented by cascading 'P' number of basic cells in series. As the number of output levels is increased the output approaches close to sinusoidal waveform. This topology contains two cascaded basic cells.

A. Operation of the Proposed Multilevel Inverter

The operation of the proposed MLI is illustrated from the switching states in table. The path of current flow is shown in Figures, for positive level and negative level respectively. Zero output voltage is represented with two switching states. Switches SIS and S25 are select switches of two respective basic cells. These switches help to add number of output levels. When all basic cells are cascaded in series, output voltages of each basic cell are added together to achieve desired output voltage across MLI.

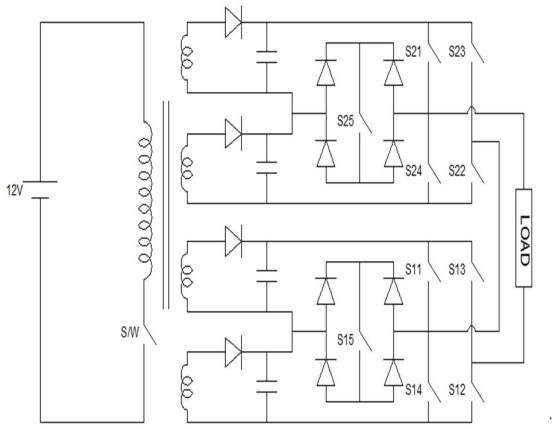

Fig 2 Circuit Diagram of the proposed 25 level inverter

TABLE II. SWITCHING STATES OF PROPOSED 25 LEVEL CONVERTER

LEVELS	S11	S12	S13	S14	S15	S21	S22	S23	S24	S25	OUTPUT VOLTAGE	OUTPUT VOLTAGE (In Per Unit)
1	0	1	0	0	0	0	1	0	0	0	0	
	0	0	1	0	0	0	0	1	0	0		
2	0	1	0	0	0	0	1	0	0	1	V21	0.08
3	0	1	0	0	0	1	1	0	0	0	V21+V22	0.16
4	0	1	0	0	1	0	0	0	0	0	V11-V21-V22	0.25
5	0	1	0	0	1	0	0	0	0	1	V11-V22	0.34
6	0	1	0	0	1	0	1	0	0	0	V11	0.42
7	0	1	0	0	1	0	1	0	0	1	V11+V12	0.5
8	0	1	0	0	1	1	1	0	0	0	V11+V12+V22	0.58
9	1	1	0	0	0	0	0	0	0	0	V11+V12-V21-V22	0.68
10	1	1	0	0	0	0	0	0	0	1	V11+V12-V22	0.76
11	1	1	0	0	0	0	1	0	0	0	V11+V12	0.84
12	1	1	0	0	0	0	1	0	0	1	V11+V12+V21	0.92
13	1	1	0	0	0	1	1	0	0	0	V11+V12+V21+V22	1
14	1	1	0	0	0	0	1	0	0	1	-V22	-0.08
15	1	1	0	0	0	0	1	0	0	0	-V21-V22	-0.16
16	1	1	0	0	0	0	0	0	0	1	V21+V22-V12	-0.25
17	1	1	0	0	0	0	0	0	0	0	V21-V12	-0.34
18	0	1	0	0	1	1	1	0	0	0	-V12	-0.42
19	0	1	0	0	1	0	1	0	0	1	-V22-V12	-0.5
20	0	1	0	0	1	0	1	0	0	0	-V21-V22-V12	-0.58
21	0	1	0	0	1	0	0	0	0	1	V21+V22-V11-V12	-0.68
22	0	1	0	0	1	0	0	0	0	0	V21-V11-V12	-0.76
23	0	1	0	0	0	1	1	0	0	0	-V11-V12	-0.84
24	0	1	0	0	0	0	1	0	0	1	-V22-V11-V12	-0.92
25	0	1	0	0	0	0	1	0	0	0	-V21-V22-V11-V12	-1

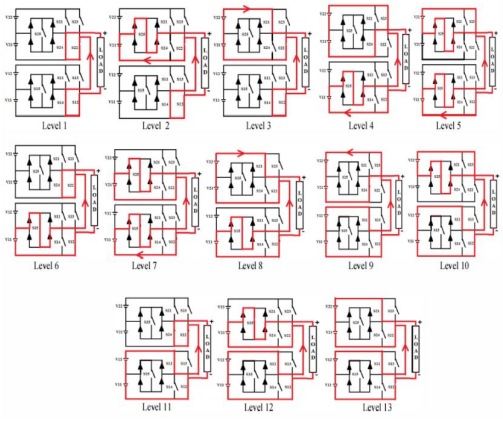

Fig 3 Current Flow Path during Positive Output Levels

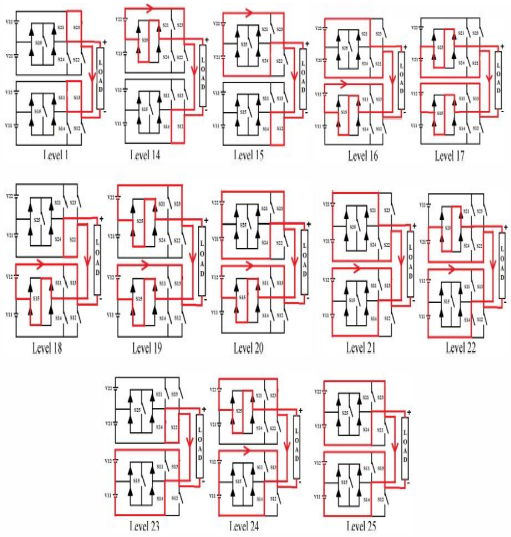

Fig 4 Current Flow Path during Positive Output Levels

The proposed converter circuit has been modeled and simulated to evaluate performance of the proposed topology. It has been modeled and simulated in MATLAB Simulink.

B. Simulation Model of the Proposed 25 Level Inverter

Simulation model of the proposed 25 level inverter is as shown. 25 output levels are obtained by using only 10 switches. This topology contains two cascaded basic cells. Each cell consists of two equal voltage sources. The voltage sources of second basic cell are in ratio of l:5 with respect to voltage sources of first basic cell. This topology helps to generate 25 output levels. An induction motor is connected as load. The THD of the output current of the motor is 4.8%. THD can be further decreased by using selective harmonic injection.

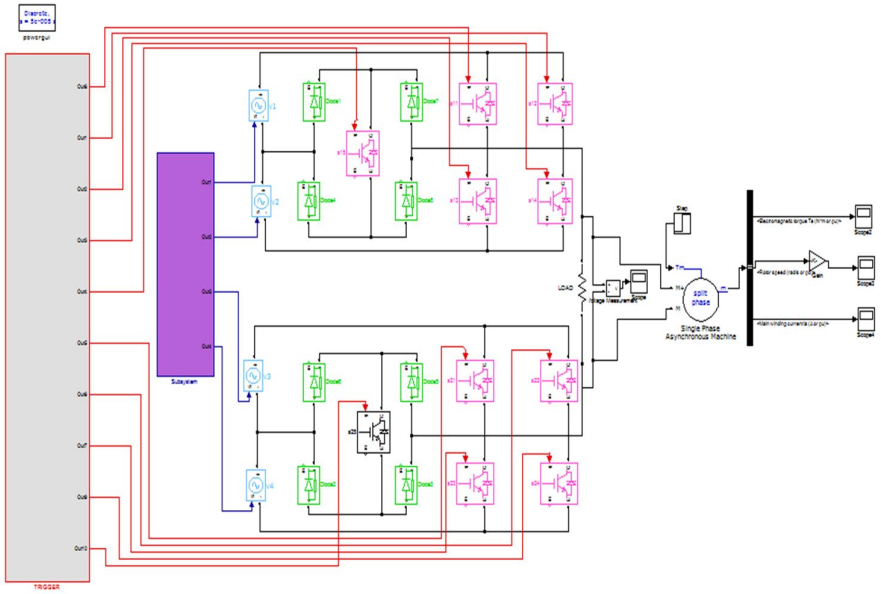

Fig 5 Simulation Model of the Proposed 25 level inverter

The switching pulses for the inverter switches are obtained by multicarrier level shifted sinusoidal pulse width modulation technique.

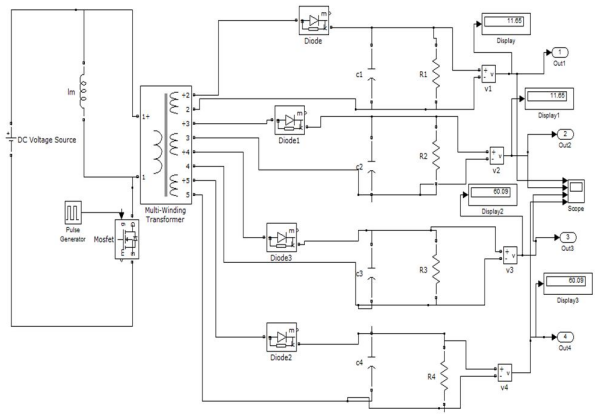

Fig 6 Simulation Model of the Flyback Converter

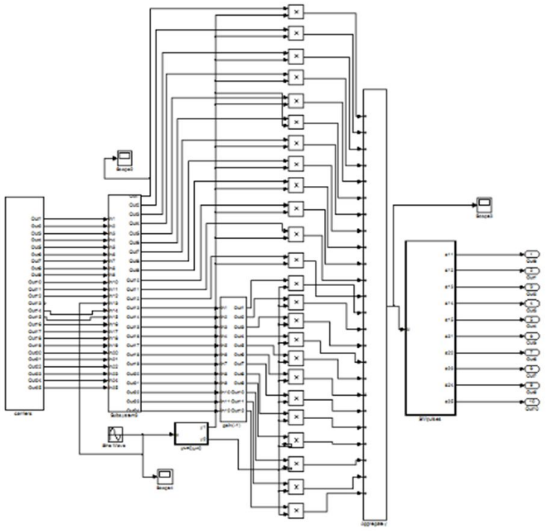

Fig 7 SPWM generation model for the proposed 25 level inverter

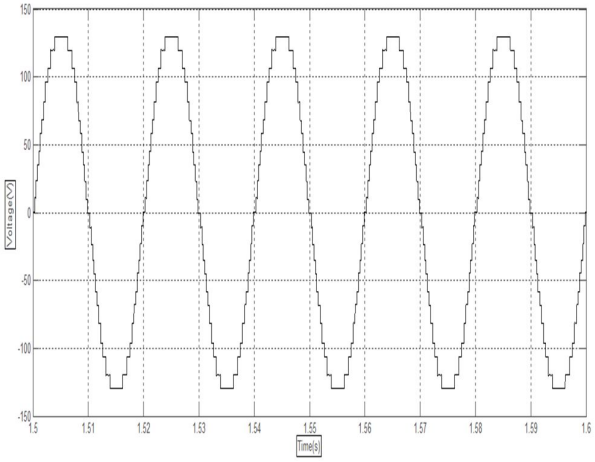

Fig 8 Output Voltage Waveform of the Proposed Converter Structure

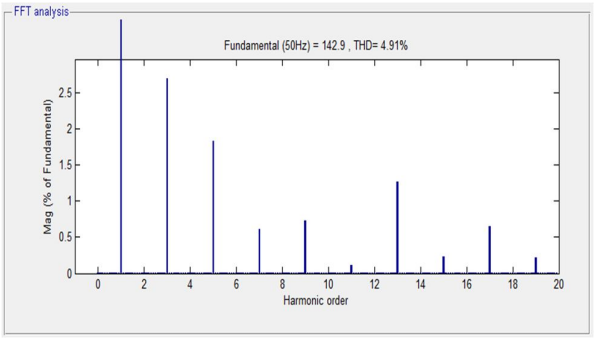

Fig 9 Harmonic Spectrum

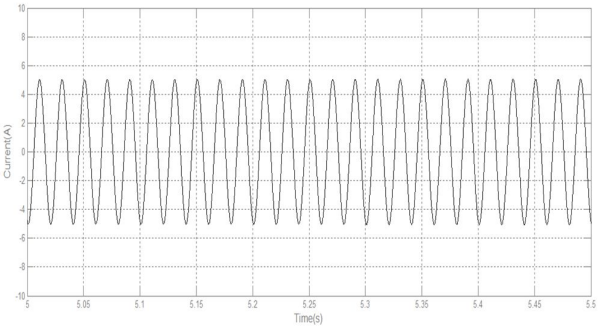

Fig 10 Output Current Waveform of the Induction Motor Load

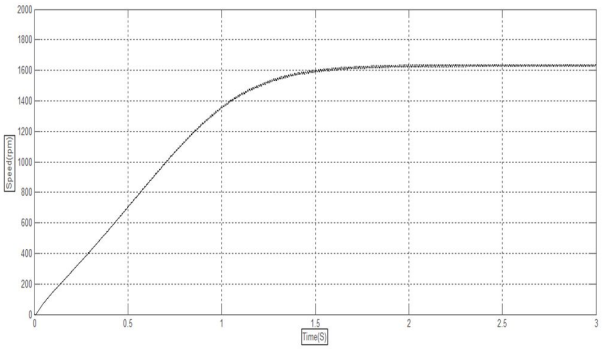

Fig 11 Speed Waveform of the Induction Motor Load

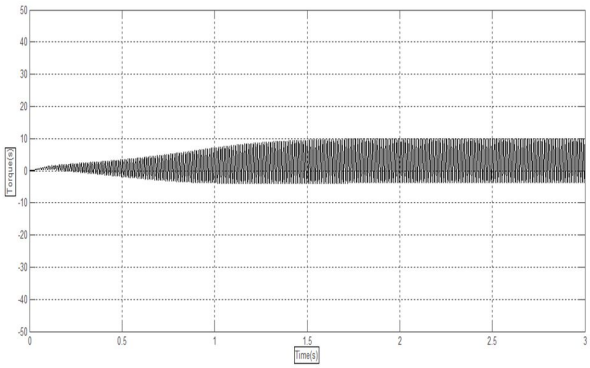

Fig 12 Torque Waveform of the Induction Motor Load

IV. Conclusion

In this project, a cascaded multilevel inverter is proposed which requires minimum number of switches with increased output levels where, output waveform is near sinusoidal. Compared with conventional multilevel inverters, it requires less number of components to achieve same number of output levels. Overall THD is very low and thus the quality of output waveform is improved. Due to the use of fewer switches, optimized circuit layout and packaging is possible. Thus less cost is required to implement the proposed inverter.

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